CLAIMS

What is claimed is:

1. Method of testing semiconductor dies, prior to their being singulated from a semiconductor wafer, comprising:

mounting a plurality of resilient contact structures directly to a plurality of terminals on a surface of a semiconductor die, said resilient contact structures each having a tip and extending from the surface of the die;

urging a substrate having a plurality of terminals towards the surface of the die to effect a plurality of pressure connections between respective terminals and tips of the resilient contact structures; and

providing signals to the terminals of the substrate to test the semiconductor die.

2. Method, according to claim 1, wherein:

the resilient contact structures are composite interconnection elements.

3. Method, according to claim 1, wherein:

the resilient contact structures are mounted by plating to the terminals of the semiconductor die.

4. Method, according to claim 1, wherein:

the resilient contact structures are anchored by a continuous overcoat to the terminals of the semiconductor die.

5. Method of testing and mounting semiconductor dies, comprising:

prior to a plurality of semiconductor dies being singulated from a semiconductor wafer:

mounting a plurality of resilient contact structures directly to a plurality of terminals on a surface of at least one of the plurality of semiconductor dies, said resilient contact structures each having a tip and extending from the surface of the die;

urging a substrate having a plurality of terminals towards the surface of the die to effect a plurality of pressure connections between respective terminals and tips of the resilient contact structures; and

providing signals to the terminals of the substrate to test the semiconductor die;

after testing the semiconductor die:

singulating the die from the wafer; and

mounting the die to an electronic component, connections being made between the resilient contact structures of the die and terminals of the electronic component.

6. Method, according to claim 5, wherein:

the resilient contact structures are composite interconnection elements.

7. Method, according to claim 5, wherein:

the electronic component is a wiring substrate.

8. Method, according to claim 5, further comprising:

prior to the plurality of semiconductor dies being singulated from a semiconductor wafer:

mounting a plurality of resilient contact structures directly to a plurality of terminals on a surface of a plurality of semiconductor dies, said resilient contact structures each having a tip and extending from the surface of the die;

urging a substrate having a plurality of terminals towards the surface of the die to effect a plurality of pressure connections between respective terminals and tips of the resilient contact structures; and

providing signals to the terminals of the substrate to test the plurality of semiconductor dies;

after testing the semiconductor dies:

singulating the dies from the wafer; and

mounting the dies to electronic components, connections being made between the resilient contact structures of the die and terminals of the electronic components.

9. Method, according to claim 8, further comprising:

mounting more than one of the dies to a single one of the electronic components.

10. Method of mounting resilient contact structures directly to semiconductor devices, comprising:

providing an insulating layer over a patterned metal layer on a surface of a semiconductor die;

providing a plurality of openings in the insulating layer;

providing a blanket conductive layer atop the insulating layer;

providing a patterned layer of masking material over the blanket conductive layer, said patterned layer of masking material having a plurality of openings aligned with the plurality of openings in the insulating layer;

bonding a wire to the blanket conductive layer within each of at least a portion of the openings in the patterned layer of masking material;

causing each bonded wire to extend from the surface of the semiconductor die;

severing each bonded wire at a distance from the surface of the semiconductor die; and

overcoating each severed wire and exposed portions of the blanket conductive layer.

11. Method, according to claim 10, further comprising:

after overcoating the severed wires, removing the masking material and selectively removing all but the previously exposed portions of the blanket conductive layer.

12. Method, according to claim 10, wherein:

the masking material is photoresist.

13. Method, according to claim 10, wherein:

the openings in the patterned layer of masking material are larger than the openings in the insulating layer.

14. Method of performing testing selected from the group consisting of test and burn-in on a semiconductor device, comprising:

mounting resilient contact structures directly to a semiconductor device;

urging the semiconductor device against a test board, said test board having contact areas, so that tips of the resilient contact structures are electrically connected to the contact areas on the test board;

performing testing on the semiconductor device;

subsequently mounting the semiconductor device to a system board, said system board having contact areas, so that the tips of the resilient contact structures are electrically connected to the contact areas on the system board.

15. Method, according to claim 14, further comprising:

permanently connecting the semiconductor device to the system board.

16. Method, according to claim 14, further comprising:

mounting the resilient contact structures to the semiconductor devices prior to singulating the semiconductor devices from a semiconductor wafer.

17. Method, according to claim 14, further comprising:

mounting the resilient contact structures to the semiconductor devices after singulating the semiconductor devices from a semiconductor wafer.

18. Method of temporarily connecting to a semiconductor device prior to permanently connecting to the semiconductor device, comprising:

mounting a plurality of electrical contact structures to a bare semiconductor device;

urging the semiconductor device against a first electronic component to effect a temporary connection between the semiconductor device and the first electronic component, with the electrical contact structures serving as an electrical interconnect between the semiconductor device and the first electronic component; and

using the same electrical contact structures mounted to the semiconductor device to effect a permanent connection between the semiconductor device and a second electronic component.

19. Method, according to claim 18, further comprising:

effecting the permanent connection by mechanically biasing the semiconductor device against the second electronic component.

20. Method, according to claim 18, further comprising:

permanently connecting the semiconductor device to the second electronic component.

21. Method, according to claim 18, wherein:

the electrical contact structures are resilient.

22. Method, according to claim 18, wherein:

the electrical contact structures are compliant.

23. Method of making a temporary connection between a first electronic component and a second electronic component, and subsequently making a permanent connection between the first electronic component and a third electronic component, comprising:

mounting a plurality of resilient contact structures to a surface of the first electronic component;

urging the first electronic component against the second electronic component to effect a temporary connection between the first electronic component and the second electronic component;

removing the second electronic component; and

mounting the first electronic component to the third electronic component.

24. Method, according to claim 23, further comprising:

while the first and second electronic components are temporarily connected, performing at least one function selected from the group consisting of burn-in and testing of the first electronic component.

25. Resilient contact structure mounted directly to a semiconductor die, comprising:

a composite interconnection element having an end attached to a semiconductor die, and extending from a surface of the semiconductor die; and

a pre-fabricated tip structure joined to the end of the composite interconnection element.

26. Resilient contact structure, according to claim 25,

wherein:

the resilient contact structure is a composite interconnection element.

27. Method of pre-fabricating tip structures for ends of contact structures extending from semiconductor dies, comprising:

depositing at least one layer of at least one conductive material on a surface of a silicon wafer;

depositing a layer of masking material atop the at least one conductive layer;

patterning openings in the masking material;

depositing at least one layer of at least one conductive material into the openings; and

removing the masking material.

28. Method, according to claim 27, further comprising:

depositing a joining material on the at least one layer of at least one conductive material previously deposited in the openings.

29. Method, according to claim 28, further comprising:

joining the tip structures to ends of contact structures.

30. Method, according to claim 29, wherein:

the contact structures are resilient contact structures.

31. Method, according to claim 29, wherein:

the contact structures are composite interconnection elements.

32. Method, according to claim 29, wherein:

the contact structures are resilient contact

structures disposed atop unsingulated semiconductor devices.

33. Method of exercising (test and/or burn-in) semiconductor devices, comprising:

fabricating a plurality of composite interconnection elements on a plurality of unsingulated semiconductor dies on a semiconductor wafer;

exercising at least a portion of the unsingulated semiconductor dies; and

singulating the semiconductor dies from the semiconductor wafer.

34. Method, according to claim 33, further comprising:

performing wafer probing prior to fabricating the plurality of composite interconnection elements.

35. Method, according to claim 33, further comprising:

performing wafer probing prior to exercising the unsingulated semiconductor dies.

36. Method, according to claim 33, wherein the step of fabricating the plurality of composite interconnection elements comprises the steps of:

depositing a blanket conductive layer onto the semiconductor die, and providing a patterned masking layer over the blanket conductive layer;

mounting elongate elements to the blanket conductive layer; and

overcoating the elongate elements with a metallic material.

37. Method, according to claim 36, further comprising:

performing wafer probing prior to mounting the elongate elements.

38. Method, according to claim 36, further comprising:

performing wafer probing prior to overcoating the elongate elements.

39. Method according to claim 33, further comprising:

singulating the semiconductor dies from the wafer.

40. Method, according to claim 39, further comprising:

performing final assembly of the singulated semiconductor dies.

41. Method of exercising (test and/or burn-in) semiconductor devices, comprising:

mounting a plurality of resilient contact structures on a plurality of unsingulated semiconductor dies on a semiconductor wafer;

exercising at least a portion of the unsingulated semiconductor dies; and

singulating the semiconductor dies from the semiconductor wafer.

42. Method of burning-in semiconductor devices, comprising:

mounting a plurality of resilient contact structures on a plurality of unsingulated semiconductor dies on a semiconductor wafer;

powering up at least a portion of the unsingulated semiconductor dies by making pressure connections to the resilient contact structures on the portion of the unsingulated semiconductor dies; and

heating the semiconductor devices to a temperature of at least 150°C for less than 60 minutes.

43. Method of making semiconductor devices, comprising:

providing terminals on a face of a semiconductor device; and

mounting free-standing resilient contact structures to the terminals.

44. Method, according to claim 43, wherein:

the resilient contact structures are hermetically sealed to the terminals.

45. Method, according to claim 43, wherein the terminals are formed by:

depositing a masking layer over a blanket conductive layer; and

providing openings in the masking layer at the desired position of each terminal.

46. Method, according to claim 45, further comprising:

providing additional openings in the masking layer, said additional openings defining portions of the blanket conductive layer which will perform a function selected from the group consisting of interconnecting two or more terminals, providing ground and/or power planes, and providing one or more capacitors directly upon the semiconductor device.